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APPLICATION FOR UNITED STATES LETTERS PATENT

Title:

METHOD OF FORMING ISOLATION FILM OF SEMICONDUCTOR DEVICE

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METHOD OF FORMING ISOLATION FILM OF SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

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Field of the Invention

The present invention relates to a method of manufacturing a semiconductor device, and more particularly, to a method of forming an isolation film in a semiconductor device by which porous silicon is formed at a portion to be insulated using electrochemical etch and porous silicon is then oxidized, using a thermal oxidation process, to form an isolation film.

Background of the Related Art

The semiconductor memory device usually employs a shallow trench isolation (hereinafter called 'STI') process as an isolation process. As the cell size is reduced due to higher integration of the semiconductor memory device, the active region and the isolation region are defined using a shallow trench isolation film.

A process of forming the shallow trench isolation film will be now described. A pad oxide film and a pad nitride film are formed on a semiconductor substrate. A photoresist pattern defining an isolation region is then formed. Next, the pad nitride film, the pad oxide film and the semiconductor substrate are etched using the photoresist pattern as an etch mask, thereby forming a trench within the semiconductor substrate.

A high density plasma (HDP) oxide film is deposited to bury the trench. At this time, the HDP oxide film is deposited in a thickness sufficient to deposit the top surface of the pad nitride film while burying the trench. Thereafter, the HDP oxide film is polished by a chemical mechanical polishing (CMP) process. The CMP process is implemented until the pad nitride film is exposed. The pad nitride film is removed. Next, an ion implantation process is performed in order to form a well junction and control the threshold voltage. The pad oxide film is then removed.

However, the above method has disadvantages that the etch process for forming the trench using plasma is difficult due to shrinkage of the trench distance, over-hang occurs at the entrance portion of the trench when the HDP oxide film is gap-filled, seam or void occurs within the trench accordingly, and reliability of the semiconductor device may be degraded since void occurs within the HDP oxide film gap-filling the trench.

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SUMMARY OF THE INVENTION

Accordingly, the present invention is contrived to substantially obviate one or more problems due to limitations and disadvantages of the related art, and an object of the present invention is to provide a method of forming isolation film in a semiconductor device by which porous silicon is formed at a portion to be insulated using electrochemical etch and porous silicon is then oxidized, using a thermal oxidation process, to form an isolation film.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent

to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as
5 the appended drawings.

To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method of forming a isolation film in a semiconductor device according to the present invention is characterized in that it comprises the steps of sequentially
10 forming a pad oxide film and a pad nitride film on a silicon substrate, forming a photoresist pattern through which an isolation region is opened, on the pad nitride film, etching the pad nitride film and the pad oxide film using the photoresist pattern as an etch mask, thus exposing the silicon substrate of the isolation region, implementing an electrochemical etch process to form porous
15 silicon in the silicon substrate of the exposed isolation region, removing the photoresist pattern, and implementing a thermal oxidization process to oxidize porous silicon, thereby forming an oxide film in the isolation region.

The electrochemical etch process is implemented using a silicon dissociation reaction in a work cell that is designed to apply a voltage to the
20 back of the silicon substrate to be used as a work electrode, in which a counterpart electrode and a reference electrode are designed so that they are immersed into an electrolyte with them kept at a given distance and an ultraviolet ray source for illuminating ultraviolet rays to the work electrode is installed on the top. A platinum electrode may be used as the counterpart

electrode. A hydrogen standard electrode may be used as the reference electrode. The electrolyte may use a solution where HF and ethanol are mixed at a given ratio. The method may further comprise the step of adding an inert gas to the electrolyte in order to prevent a hydrogen gas occurring during the dissociation reaction of silicon from hindering the silicon dissociation reaction. The voltage is 1.5V ~ 8V.

The thermal oxidization process is implemented using a wet oxidization mode at a temperature of 700 ~ 900°C under O₂ and H₂ atmosphere

In another aspect of the present invention, it is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be apparent from the following detailed description of the preferred embodiments of the invention in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates a work cell for performing an electrochemical etch process according to a preferred embodiment of the present invention;

FIG. 2 ~ FIG. 5 illustrate semiconductor devices for explaining a method of forming porous silicon through electrochemical etch and then thermally oxidizing porous silicon to form an isolation film according to a preferred embodiment of the present invention; and

FIG. 6 is a SEM (scanning electron microscope) photograph showing porosities formed in the silicon substrate through electrochemical etch.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

5 Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

 The present invention relates to a method of forming porosities through
10 an electrochemical etch process to form an isolation film. The isolation film may be formed by forming porous silicon at a portion to be insulated using the electrochemical etch process and oxidizing porous silicon using a thermal oxidation process.

 FIG. 1 illustrates a work cell for performing an electrochemical etch
15 process according to a preferred embodiment of the present invention. FIG. 2 ~ FIG. 5 illustrate semiconductor devices for explaining a method of forming porous silicon through electrochemical etch and then thermally oxidizing porous silicon to form an isolation film according to a preferred embodiment of the present invention. FIG. 6 is a SEM (scanning electron microscope)
20 photograph showing porosities formed in the silicon substrate through electrochemical etch, which shows 'A' portion in FIG. 4.

 Referring to FIG. 1, a work cell 120 for performing the electrochemical etch process in order to form porosities, is designed to apply a voltage (V) to the back of a wafer (W) to be used as a work electrode. A counterpart

electrode 130 and a reference electrode 140 are designed so that they are immersed into the electrolyte 160 with them kept at a given distance. Also, an ultraviolet ray source 150 is located on the work cell 120 so that the ultraviolet rays 152 could be illuminated on the work electrode. The voltage
5 (V) applied to the word electrode, i.e., the wafer (W) is about 1.5V ~ 8V.

By reference to FIG. 2, a pad oxide film 102 and a pad nitride film 104 are sequentially formed on a silicon substrate 100. The pad oxide film 102 is formed in thickness of about 50~1000 Å and the pad nitride film 104 is formed in thickness of about 500~1500 Å. A photoresist pattern 106
10 defining an isolation region is formed on the pad nitride film 104.

With reference to FIG. 3, the pad nitride film 104 and the pad oxide film 102 are etched using the photoresist pattern 106 as an etch mask, thereby exposing the silicon substrate 100 at a portion where an isolation region will be formed. The wafer (W) prepared as above is mounted on the work cell
15 120 and is then experienced by an electrochemical etch process.

Turning to FIG. 1 and FIG. 4, the method of forming the isolation film according to the preferred embodiment of the present invention employs porosity formation by the electrochemical etch process. The process of forming the porosity is performed using a solution where 49% HF and ethanol
20 are mixed as an electrolyte 160 while the ultraviolet rays 152 of a given wavelength are illuminated using the ultraviolet ray source 150. The work electrode used in the electrochemical etch process is the silicon wafer (W), a hydrogen standard electrode is used as the reference electrode 140 and a platinum electrode is used as the counterpart electrode 130. Reactive

activation energy necessary for a dissociation reaction of silicon is supplied by applying the voltage (V) by which silicon could be dissociated to the work electrode. In order to prevent hindrance of the silicon dissociation reaction by generation of a hydrogen gas when the silicon dissociation reaction occurs,
5 the hydrogen gas is removed from the reaction surface by adding an inert gas such as argon (Ar) to the electrolyte 16 and then bobbling it.

A dissociation mechanism for electrochemical etch of silicon is as follows.

A silicon surface that reacts to the electrolyte 160 where HF and ethanol
10 are mixed does not have a hole (h^+) since it is saturated with H atoms. The silicon surface is inert against attack of F^- ion. This is because an atmosphere that F^- ion can react is not prepared since there is no significant difference in the electronegativity between 2.2, the electronegativity of H and 1.9, the electronegativity of Si. If the hole (h^+) is supplied by the ultraviolet rays
15 illuminated on the silicon surface, nucleophilic attack of the F^- ion is made possible since the electronegativity of Si is relatively lowered compared to the H atoms.

In case of n type silicon, creating of the hole on the silicon surface is an important step to induce a dissociation procedure of silicon. If H is
20 substituted with F, the electronegativity of Si is further lowered and attack of F^- continuously occurs.

Hydrogen is generated by a series of reaction, partial dissociation occurs on the silicon surface by continuous attack of F^- and a new surface is thus created. This change causes to vary distribution of an electric field on the

silicon surface. As the hole is supplied from a bulk region of silicon to a portion where silicon is dissociated by this change of the electric field, the trench is formed in a vertical direction parallel to a direction along which the hole is supplied. Porosities are formed at the silicon substrate 100 being a region where the isolation region will be formed through this electrochemical etch.

When silicon exists under a positive bias (V) in a dilute HF solution, a current to voltage characteristic region where the porosities may be formed is a low voltage. Electrical polishing occurs at a high voltage. Both the reaction where the porosities are formed and an electrical polishing reaction occur at the intermediate region (transfer region) since silicon and HF reacts. Accordingly, the most important thing in the dissociation procedure of silicon when the voltage by which the porosities may be formed is applied to silicon, is the hole (h^+) being a carrier. This hole decides a dissociation speed of silicon. What the ultraviolet rays are illuminated when the silicon wafer is electrically chemically etched, is to sufficiently supply the holes to the space charge layer of the silicon surface so that the dissociation reaction can start in the step where silicon begins to dissociate.

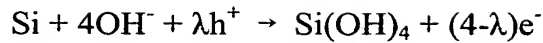
The porosities could be formed through the following reaction equation 1.

【Reaction Equation 1】

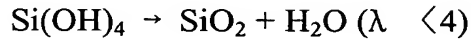


The electrical polishing reaction is generated through the following reaction equations 2 and 3.

【Reaction Equation 2】



【Reaction Equation 3】



5 In case where the porosities are formed by the electrical chemical etch method of the present invention, parameters that control the size of the porosity include the concentration of the electrolyte (volume ratio of HF and ethanol), the intensity of a voltage applied to the work electrode, reaction time, the intensity of the ultraviolet ray source, and the like. Furthermore,
10 parameters that control the depth of the porosity include the intensity of the voltage applied and reaction time. The size and depth of the porosity could be controlled and the number of the porosity (degree of the porosity) for a given area could be controlled, using these parameters.

Referring to FIG. 5, the photoresist pattern is removed. At this time,
15 the photoresist pattern may be removed under an O₂ atmosphere by means of an ashing process. After porous silicon is formed through electrochemical etch, a thermal oxidization process is performed to form an oxide film. At this time, the thermal oxidization process may employ a wet oxidization mode. The thermal oxidization process is implemented at a temperature of about
20 700~900°C under O₂ and H₂ atmosphere. As such, if porous silicon is oxidized by the thermal oxidization process after porous silicon is formed through electrochemical etch, O₂ or H₂O being an oxidizing agent is diffused into the Si/SiO₂ interface where Si reacts to H₂O or O₂ to form SiO₂. Therefore, as silicon is consumed while the oxide film is grown, both the

porosity and silicon could be formed to be the oxide film by controlling the size of the porosity and the degree of the porosity. If porous silicon is formed to be the oxide film by this method, it could be used as the isolation film of the semiconductor device.

5 As described above, the conventional process of forming the isolation film had problems that the trench etch process using plasma is difficult due to shrinkage of the trench distance, over-hang occurs at the entrance portion of the trench when the HDP oxide film is gap-filled, seam or void occurs within the trench accordingly, and reliability of the semiconductor device may be
10 degraded since void occurs within the HDP oxide film that gap-fills the trench.

 As described above, however, the present invention has a new effect that it can significantly simplify the process compared to a conventional isolation film formation process since the isolation film of the semiconductor device can be formed by a photolithography process, a process of etching the
15 pad nitride film and the pad oxide film, an electrochemical etch process (porosity formation process) and the thermal oxidization process. Also, the present invention has advantageous effects that it can solve difficulty plasma etch depending on integration of the semiconductor device and a problem that void is formed within the HDP oxide film.

20 Furthermore, according to the present invention, the isolation film is formed on a silicon wafer surface. Therefore, the present invention has a new effect that it can prevent a phenomenon that a gate oxide film is made thin due to a moat generated in a conventional isolation film process.

 The forgoing embodiments are merely exemplary and are not to be

construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those
5 skilled in the art.